**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

Claim 1 (currently amended): A stacked gate vertical flash memory, comprising:

a semiconductor substrate with a trench;

a source conducting layer, formed on a bottom of the trench;

an insulating layer, formed on the source conducting layer;

a gate dielectric layer, formed on a sidewall of the trench;

a ~~conducing~~ conducting spacer, formed on the gate dielectric layer as a floating gate, wherein the conducting spacer is tapered to a point at the gate dielectric layer;

an inter-gate dielectric layer, covered on the conducting spacer; and

a conducting control gate filled in the trench.

Claim 2 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the source conducting layer comprises a polysilicon layer or an epi-silicon layer

Claim 3 (original): The stacked gate vertical flash memory as claimed in claim 2, wherein the source conducting layer is a doped As ion layer.

Claim 4 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the source conducting layer can be a common source.

Claim 5 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the insulating layer comprises an oxide layer.

Claim 6 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the gate dielectric layer comprises a gate oxide layer.

Claim 7 (canceled)

Claim 8 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the conducting spacer comprises a polysilicon layer or an epi-silicon layer.

Claim 9 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the inter-gate dielectric layer comprises a gate oxide layer.

Claim 10 (original): The stacked gate vertical flash memory as claimed in claim 1, wherein the second conducting layer comprises a polysilicon layer or an epi-silicon layer.

Claim 11 (original): The stacked gate vertical flash memory as claimed in claim 1, further comprises a source area formed on a side of the insulating layer in the semiconductor substrate, wherein the source comprises an As ion implanted area.

Claim 12 (original): The stacked gate vertical flash memory as claimed in claim 1, further comprises a drain area formed on a side of the top of the conducting spacer in the semiconductor substrate, wherein the drain comprises an As ion implanted area.

Claim 13 (original): The stacked gate vertical flash memory as claimed in claim 1 further comprises an isolation oxide layer for separating the source conducting layer and the semiconductor substrate.

Claim 14 (currently amended): A stacked gate vertical flash memory, comprising:

a semiconductor substrate with a trench, wherein an isolation layer is formed on a bottom of the trench;

a source conducting layer, formed on the bottom of the trench, wherein the source conducting layer and the semiconductor substrate are separated by the isolation layer;

an insulating layer, formed on the source conducting layer, wherein the insulating layer and others formed thereon are separated by the insulating layer;

a gate dielectric layer, formed on a sidewall of the trench;

a ~~conducing~~ conducting spacer, formed on the gate dielectric layer as a floating gate, wherein the conducting spacer is tapered to a point at the gate dielectric layer;

a source area, formed on a side of the insulating layer in the semiconductor substrate~~, wherein the conducting spacer electrically connected to the source conducting layer and the conducting spacer~~;

a drain area, formed on a side of a top of the conducting spacer;

an inter-gate dielectric layer, covered on the conducting spacer; and

a control gate conducting filled in the trench.

Claim 15 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer comprises a polysilicon layer or an epi-silicon layer

Claim 16 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer is an As ion doped layer.

Claim 17 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the insulating layer comprises an oxide layer.

Claim 18 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the gate dielectric layer comprises a gate oxide layer.

Claim 19 (canceled)

Claim 20 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the conducting spacer comprises a polysilicon layer or an epi-silicon layer.

Claim 21 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer can be an As ion doped layer.

Claim 22 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the drain conducting layer can be an As ion doped layer.

Claim 23 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the inter-gate dielectric layer comprises a gate oxide layer.

Claim 24 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the control gate conducting layer comprises a polysilicon layer or an epi-silicon layer.

Claim 25 (original): The stacked gate vertical flash memory as claimed in claim 14, wherein the isolation layer comprises an oxide layer.

Claims 26-33 (canceled)